Amendments to the Specification

Please replace the paragraph on page 1, lines 7-10 with the following paragraph:

1. United States patent application entitled, "Error Insertion Circuit for SONET Forward Error Correction," ~~attorney docket no.: M-8353-US~~ Serial No. 09/821,948, naming Andrew J. Thurston and Douglas Duschatko as inventors and filed ~~substantially contemporaneously with the present application~~ March 30, 2001;

Please replace the paragraph on page 1, lines 11-14 with the following paragraph:

2. United States patent application entitled, "BCH Forward Error Correction Decoder", ~~attorney docket no.: M-8342-US~~ Serial No. 09/822,950, naming Andrew J. Thurston as inventor and filed ~~substantially contemporaneously with the present application~~ March 30, 2001; and

Please replace the paragraph on page 1, lines 15-18 with the following paragraph:

3. United States patent application entitled, ~~"Automatic generation of hardware description language code for COMPlex polynomial functions"~~ "Automatic Generation of Hardware Description Language Code for Complex Polynomial Functions", ~~attorney docket no.: M-8319-US~~ Serial No. 09/822,713, naming Andrew J. Thurston and Douglas Duschatko as inventors and filed ~~substantially contemporaneously with the present application~~ March 30, 2001.

Please insert the following paragraphs on page 10, between lines 12 and 13:

Figure 12 illustrates a state machine and multiple Galois field multiply accumulators.

Figure 13 illustrates a Galois field unit.